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Product information

To:

Product Name: M133NWN1 R3

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| | Revised Record | | | | | | | | | | |
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| Ver. | Date | Revised Content/Summary | Page | Revised By | | | | | | | |
| 01 | 2012/11/28 | Tentative | All | 魏工钧 | | | | | | | |
| 02 | 2013/03/04 | Change lable HW:1.1 into HW:1.2 | 29 | 谢龙 | | | | | | | |
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1.0 General Descriptions

1.1 Introduction

The M133NWN1 R3 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT-LCD has a 13.3-inch diagonally measured active display area with HD resolution (1,366 horizontal by 768 vertical) pixel arrays.

1.2 Features

- 13.3" TFT-LCD Panel
- Supported HD 1,366x768 pixels resolution
- Compatible with RoHS standard
- Supported eDP1.2 Electrical Interface

1.3 Product Summary

| Items | Specifications | Unit |
|------------------------------|-----------------------------------|--------------------|
| Screen Diagonal | 13.3" | Inch |
| Active Area | 293.4168 (H) x 164.9664 (V) | mm |
| Pixels (H x V) | 1,366 (RGB) x 768 | - |
| Pixel Pitch | 0.2148(H)×0.2148(V) | mm |
| Pixel Arrangement | R.G.B. Vertical Stripe | - |
| Display Mode | TN, Normally White | - |
| White Luminance | 200 (Typ.) | cd /m ² |
| Response Time | 8 (Typ.), 16 (Max.) | msec |
| Input Voltage | 3.3±0.3 | V |
| Power Consumption | 2.5 (Max.) | W |
| Weight | 260(Max) | g |
| Outline Dimension | 306.8(Max.)x189.2(Max.)x3.0(Max.) | mm |
| Electrical Interface (Logic) | eDP1.2 | - |
| Support Color | 262 K | - |
| NTSC | 45 | % |
| Optimum Viewing Direction | 6 o'clock | - |
| Thickness | 3.0(Max.) | mm |
| Surface Treatment | AG,3H | - |



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1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

PCB Timing Controller eDP Receiver eDP **TFTLCD** 1366(R/G/B) X768 LDO DC Source Driver IC Power **LED** PWM IC **LED Light Bar Power**

Figure 1 Block Diagram

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2.0 Absolute Maximum Ratings

Table 1 Electrical Absolute Rating

| Item | Symbol | Min. | Max. | Unit | Note | |
|---------------------------------|----------------|--------|-------|------|---------|--|
| Logic Supply Voltage | V_{DD} | (-0.3) | (6.0) | V | | |
| Supply V _{LED} Voltage | V_{LED} | (-0.3) | (24) | V | (1),(2) | |
| LED Reverse Voltage | V_R | - | (5) | V | (1),(2) | |
| LED Forward Current | I _F | - | (30) | mA | | |

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Operating temperature 25°C, humidity 55%.

Table 2 Absolute Ratings of Environment

| Item | Symbol | Min. | Max. | Unit | Conditions | | | |
|--------------------------|--------|------|------|--------------|-------------|--|--|--|
| Operating Temperature | TOP | 0 | 50 | $^{\circ}$ C | | | | |
| Operating Humidity | HOP | 10 | 80 | %RH | (4) (2) (2) | | | |
| Storage Temperature | TST | -20 | 60 | $^{\circ}$ | (1),(2),(3) | | | |
| Storage Humidity | HST | 10 | 90 | %RH | | | | |
| Vibration(non-operating) | Vnop | - | 1.5 | G | (4) | | | |
| Shock(non-operating) | Snop | - | 210 | G | (5) | | | |

Note (1) Maximum Wet-Bulb temperature should be 39 ℃. No condensation of water.

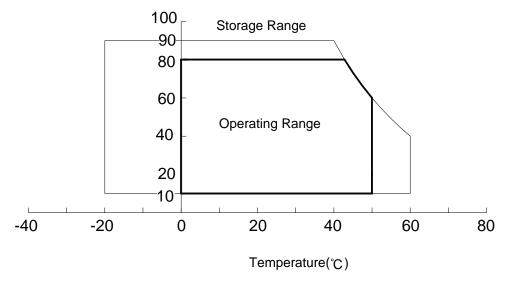
- (2) When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module is less than 60 ℃.
- (3) Storage /Operating temperature:



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Figure 2 Absolute Ratings of Environment of the LCD Module

Relative Humidity(%RH)



- (4) 10-200Hz, random vibration, 30 min for X, Y, Z axis.
- (5) 3ms, half sine wave, one time for X, Y, Z axis.

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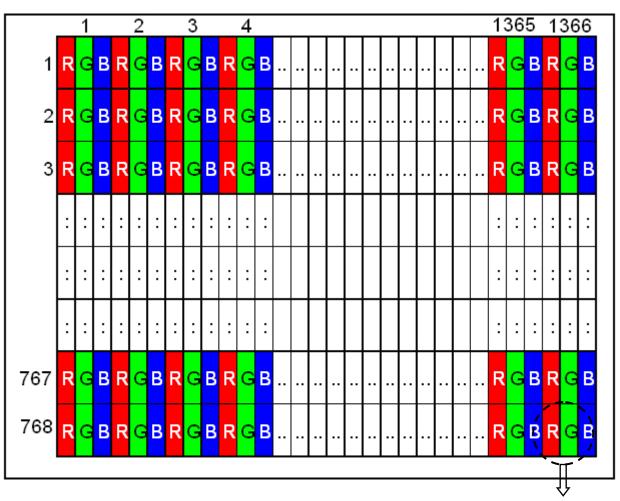
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3.0 Pixel Format Image

Figure 3 shows the relationship of the input signals and LCD pixel format image.

Figure 3 Pixel Format



R+G+B dots=1 pixel

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4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 3 Optical Characteristics

| Item | Condition | s | Min. | Тур. | Max. | Unit | Note | | | | |
|----------------------|------------------|----|-------|---------|-------|--------|-------------|--|--|---|---------|
| | Horizontal | θ∟ | - | 45 | - | | | | | | |
| Viewing Angle | Honzontai | θR | - | 45 | - | dograe | (4) (2) (2) | | | | |
| (CR>10) | Vertical | θт | - | 20 | - | degree | (1),(2),(3) | | | | |
| | vertical | θв | - | 40 | - | | | | | | |
| Contrast Ratio | Center | | 400 | 500 | - | - | (1),(2),(4) | | | | |
| | Rising | | - | 3 | - | ms | | | | | |
| Response Time | Falling | | - | 5 | - | ms | (1),(2),(5) | | | | |
| | Rising + Falling | g | - | 8 | 16 | ms | | | | | |
| | Red x | | | (0.593) | | - | | | | | |
| | Red y Green x | | | (0.345) | +0.03 | - | | | | | |
| | | | -0.03 | (0.319) | | ı | | | | | |
| Color Chromaticity | Green y | | -0.03 | (0.592) | +0.03 | - | (1) (2) | | | | |
| (CIE1931) | Blue x | | | (0.153) | | | | | | - | (1),(2) |
| | Blue y | | | (0.119) | | ı | | | | | |
| | White x | | 0.283 | 0.313 | 0.343 | - | | | | | |
| | White y | | 0.299 | 0.329 | 0.359 | - | | | | | |
| NTSC | - | | - | 45 | - | % | - | | | | |
| White Luminance | - | | 170 | 200 | - | cd/m^ | (4) (2) (6) | | | | |
| | | | | | | 2 | (1),(2),(6) | | | | |
| Luminanaa Uniformitu | 5Points | | 80 | - | - | % | (4) (2) (7) | | | | |
| Luminance Uniformity | 13Points | | 60 | - | - | % | (1),(2),(7) | | | | |

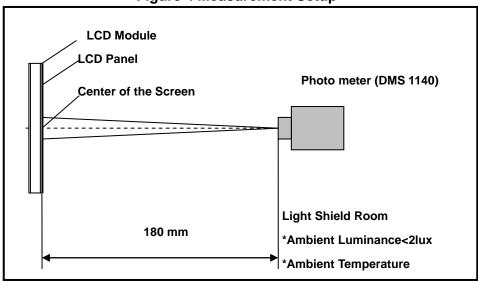
Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature (25°C) for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



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Figure 4 Measurement Setup



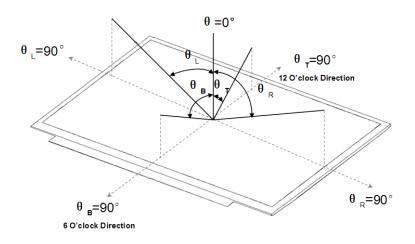
Note (2) The LED input parameter setting as:

V_LED: 12V (±0.1V)

PWM_LED: duty 100 %

Note (3) Definition of Viewing Angle

Figure 5 Definition of Viewing Angle



Note (4) Definition Of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression Contrast Ratio (CR) = L63 / L0

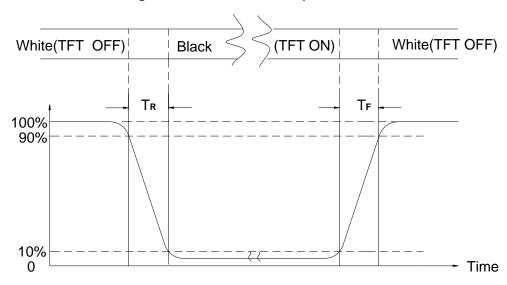
L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (5) Definition Of Response Time (TR, TF)



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Figure 6 Definition of Response Time



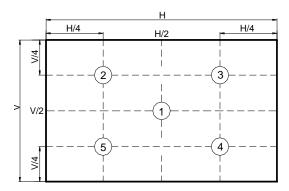
Note (6) Definition Of Luminance White:

Measure the luminance of gray level 63 at center point (Ref: Active area)

Display Luminance= (L1+L2+L3+L4+L5) /5

H—Active area length V—Active area width L—Luminance

Figure 7 Measurement Locations Of 5 Points



Note (7) Definition Of Luminance Uniformity (Ref: Active area)

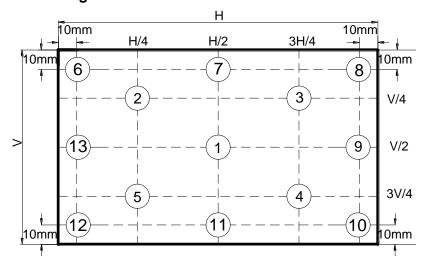
Measure the luminance of gray level 63 at 5 points and 13 points.

| Luminance Uniformity(5 Points)= | Minimum Brightness of Five Points × 100 % |
|--|---|
| Editinated of morning (o'r oints) | Maximum Brightness of Five Points |
| Luminance Uniformity(13 Points)= | Minimum Brightness of Thirteen Points × 100 % |
| Editinative officiality (10 1 offics)= | Maximum Brightness of Thirteen Points⊌ |



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Figure 8 Measurement Locations Of 13 Points



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5.0 Backlight Characteristics

5.1 Parameter Guideline Of LED Backlight

Table 4 Parameter Guideline for LED Backlight

| Item | Symbol | | Min. | Тур. | Max. | Units | Note |
|-----------------------|---------------------|------|--------|------|-------|-------|---------|
| LED Input Voltage | V _{LED} | | 5 | 12 | 21 | V | |
| LED Power | D | | | | 1.65 | W | |
| Consumption | P _{LED} | | - | • | 1.65 | VV | |
| LED Forward Voltage | V _F | | 2.7 | 3 | 3.1 | V | |
| LED Forward Current | I _F | | - | 16 | - | mA | (0) |
| PWM Signal Voltage | V | High | 2.0 | 3.3 | 3.6 | V | (2) |
| Pyvivi Signai voitage | V_{PWM_EN} | Low | - | - | 0.5 | V | |
| LED Enable Voltage | V | High | 2.0 | 3.3 | 3.6 | V | |
| LED Enable voltage | V _{LED_EN} | Low | - | ı | 0.5 | V | |
| Input PWM Frequency | FPWM | | 200 | - | 1,000 | Hz | |
| Duty Ratio | PWM | | 1 | - | 100 | % | |
| LED Life Time | LT | | 15,000 | 1 | - | Hours | (1),(2) |

Note (1) The LED life time define as the estimated time to 50% degradation of initial luminous.

Note (2) Operating temperature 25 ℃, humidity 55%.

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6.0 Electrical Characteristics

6.1 Interface Connector

Table 5 Connector Name / Designation

| Manufacturer | STM (信盛) |
|-------------------------------|--------------|
| Type / Part Number | SMAK24025P30 |
| Mating Receptacle/Part Number | PK24025P30 |

Table 6 Signal Pin Assignment

| Pin # | Signal Name | Description | Remarks |
|-------|---------------|-------------------------------------|-------------|
| 1 | DCR | DCR Enable | - |
| 2 | H_GND | High Speed Ground | - |
| 3 | LAN1_N | Complement Signal Link Lane 1 | - |
| 4 | LAN1_P | True Signal Link Lane 1 | - |
| 5 | H_GND | High Speed Ground | - |
| 6 | Lane 0_N | Complement Signal Link Lane 0 | - |
| 7 | Lane 0_P | True Signal Line 0 | - |
| 8 | H_GND | High Speed Ground | - |
| 9 | AUX_CH_P | True Signal Auxiliary Ch. | - |
| 10 | AUX_CH_N | Complement Signal Auxiliary Ch. | - |
| 11 | H_GND | High Speed Ground | - |
| 12 | LCD_VCC | LCD Logic and Driver Power | +3.3V |
| 13 | LCD_VCC | LCD Logic and Driver Power | +3.3V |
| 14 | LCD Self-test | LCD Panel Self-test Enable | - |
| 15 | LCD_GND | LCD logic and driver Ground | - |
| 16 | LCD_GND | LCD logic and driver Ground | - |
| 17 | HPD | HPD Signal Pin | - |
| 18 | BL_GND | Backlight Ground | - |
| 19 | BL_GND | Backlight Ground | - |
| 20 | BL_GND | Backlight Ground | - |
| 21 | BL_GND | Backlight Ground | - |
| 22 | BL_ENABLE | Backlight On/Off enable | +3.3V |
| 23 | BL_PWM_DIM | System PWM Signal Input for Dimming | +3.3V Swing |
| 24 | NC | Reserved | - |
| 25 | NC | Reserved | - |
| 26 | BL_PWR | Backlight Power | +12V |
| 27 | BL_PWR | Backlight Power | +12V |
| 28 | BL_PWR | Backlight Power | +12V |



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| 29 | BL_PWR | Backlight Power | +12V |
|----|--------|-----------------|------|
| 30 | NC | Reserved | - |

Note: All input signals shall be low or Hi- resistance state when VDD is off.

6.2 Signal Electrical Characteristics

Table 7 Display Port Main Link

| Parameter | Description | | Тур. | Max. | Unit |
|-------------------------------|---|------|------|------|------|
| V _{CM} | Differentia Common Mode Voltage | TBD | (0) | TBD | V |
| V _{Diff P-P} Level 1 | Differential Peak to Peak Voltage Level 1 | 0.34 | 0.40 | 0.46 | V |
| V _{Diff P-P} Level 2 | Differential Peak to Peak Voltage Level 2 | 0.51 | 0.60 | 0.68 | V |
| V _{Diff P-P} Level 3 | Differential Peak to Peak Voltage Level 3 | 0.69 | 0.80 | 0.92 | V |
| V _{Diff P-P} Level 4 | Differential Peak to Peak Voltage Level 4 | 1.02 | 1.20 | 1.38 | V |

Note: (1) Input signals shall be low or High-impedance state when VDD is off.

- (2) It is recommended to refer the specifications of VESA Display Port Standard V1.1a in detail.
- (3) Fallow as VESA display port standard V1.1a at both 1.62 and 2.7Gbps link rates.

Figure 9 Display Port Main Link Signal

Figure 10 Display Port AUX_CH Signal

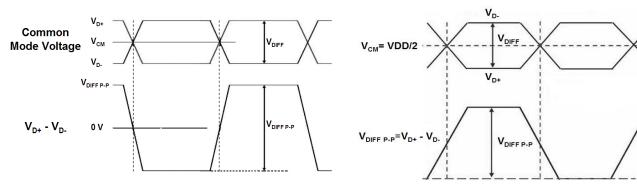


Table 8 Display Port AUX_CH

| Parameter | Description | Min. | Тур. | Max. | Unit |
|-----------------------|-----------------------------------|------|-------|------|------|
| V _{CM} | Differentia Common Mode Voltage | 0 | VDD/2 | 2 | V |
| V _{Diff P-P} | Differential Peak to Peak Voltage | 0.39 | - | 1.38 | V |

Note: Fallow as VESA display port standard V1.1a.

Table 9 Display Port V_{HPD}

| Parameter | Description | Min. | Тур. | Max. | Unit |
|-----------|-------------|------|------|------|------|
| V_{HPD} | HPD Voltage | 2.25 | - | 3.60 | V |

Note: Fallow as VESA display port standard V1.1a.



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Figure 11 Display Port Interface Power Up/Down Sequence, Normal System Operation (Reference)

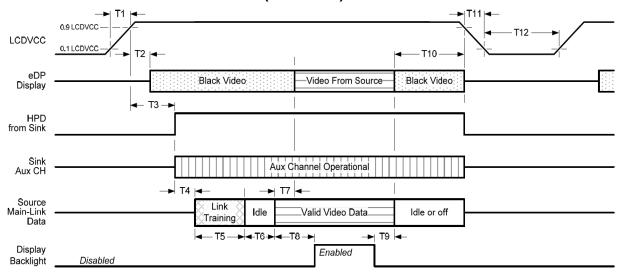
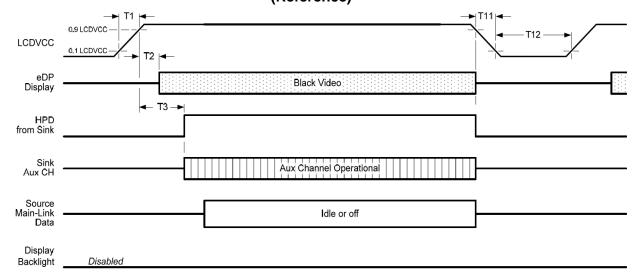


Figure 12 Display Port Interface Power Up/Down Sequence, Aux Channel Transaction Only (Reference)



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Table 10 eDP Panel Power Sequence Timing Parameters (Reference)

| Timing | Decembration | Reqd. | Lin | nits | Natas |
|-----------|---|--------|---------|-----------|--|
| Parameter | Description | Ву | Min. | Max. | Notes |
| T1 | Power rail rise time, | Source | 0.5 | 10 | - |
| | 10% to 90% | | ms | ms | |
| T2 | Delay from LCD VCC to black video generation | Sink | 0 ms | 200 ms | Prevents display noise until valid video data is received from the Source.(see note 1 below) |
| Т3 | Delay from LCD VCC to | Sink | 0 ms | 200 ms | Sink Aux Channel must be operational upon HPD high. |
| Т4 | Delay from HPD high to link training initialization | Source | - | - | Allows for Source to read Link capability and initialize. |
| T5 | Link training duration | Source | - | - | Dependant on Source link training protocol. |
| T6 | Link idle | Source | - | - | Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization. |
| Т7 | Delay from valid video data from Source to video on display | Sink | 0 ms | 50 ms | Max allows Sink validate video data and timing. |
| Т8 | Delay from valid video from Source to backlight enable | Source | - | - | Source must assure display video is stable. |
| Т9 | Delay from backlight disable to end of valid video data | Source | - | - | Source must assure backlight is no longer illuminated.(see note 1 below) |
| T10 | Delay from end of valid video data from Source to power off | Source | 0 ms | 500 ms | - |
| T11 | Power rail fall time, 90% to 10% | Source | - | 10 ms | - |



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| T12 Power off time |
|--------------------|
|--------------------|

Note (1): The Sink must include the ability to generate black video autonomously. The Sink must automatically enable black video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)
- When no Main Link data, or invalid video data, is received from the Source. Black video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note (2): The Sink may implement the ability to disable the black video function, as described in Notes (1)above, for system development and debugging purposes.

Note (3): The Sink must support Aux Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to respond to an Aux Channel transaction with the time specified within T3 max.



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7.0 **Interface Timings**

7.1 Timing Characteristics

Basically, interface timings should match the 1366 x 768 /60Hz manufacturing guide line timing.

Table 11 Interface Timings

| Parameter | Symbol | Unit | Min. | Тур. | Max. |
|------------------------|-------------------|--------|-------|-------|-------|
| Signal Clock Frequency | f _{dck} | MHz | 47.32 | 73.81 | 86.60 |
| Frame Rate | V _{sync} | Hz | 55 | 60 | 65 |
| H Total Time | T_{hp} | clocks | 1520 | 1532 | 1606 |
| H Active Time | HA | clocks | | 1366 | |
| H Blanking | T_{hfp} | clocks | - | 166 | - |
| V Total Time | T _{vp} | lines | 778 | 803 | 830 |
| V Active Time | VA | lines | 768 | | |
| V Blanking | T_{vfp} | lines | - | 35 | - |

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8.0 Power Consumption

Input power specifications are as follows.

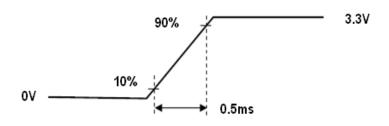
Table 12 Power Consumption

| Item | | Symbol | Min. | Тур. | Max. | Units | Note |
|----------------|---------------|----------|------|-------|-------|-------|----------|
| Logic/LCD Dri | ve Voltage | VDD | 3.0 | 3.3 | 3.6 | V | (3), (4) |
| VDD Current | Black Pattern | IDD | 1 | 0.258 | 0.283 | Α | (1) (1) |
| VDD Power C | onsumption | PDDBlack | - | - | 0.85 | W | (1),(4) |
| Rush Current | | Irush | - | ı | 1.5 | Α | (2),(4) |
| Allowable Log | ic/LCD | VDDrp | | | 200 | mV | (4) |
| Drive Ripple V | oltage/ | VOOIP | - | | 200 | 1117 | (4) |

Note (1) IDD $_{Black}$ measurement condition f_{clk} =75.40 MHz, f_{v} =60Hz, VDD=3.3V, Black pattern.

Note (2) Measure Condition

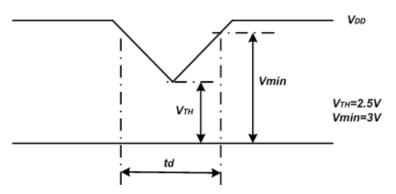
Figure 13 VDD rising time



VDD rising time

Note (3) VDD Power Dip Condition

Figure 14 VDD Power Dip



If V_{TH}<V_{DD}≤Vmin, then t_d≤10ms; when the voltage return to normal our panel must revive



| | | | | , , , , , , , , , , , , , , , , , , , | | |
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automatically.

Note (4) Operating temperature 25 $^{\circ}$ C, humidity 55%.



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9.0 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD is off.

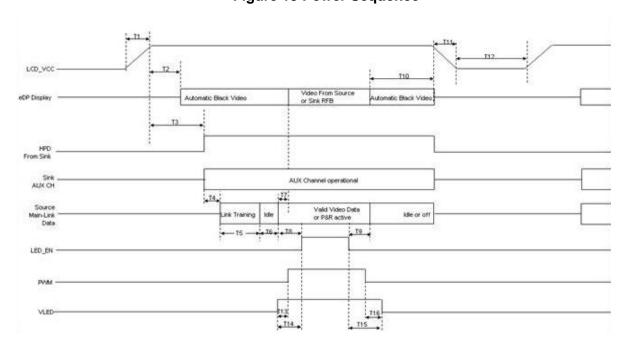


Figure 15 Power Sequence

Table 13 Power Sequencing Requirements

| Parameter | Unit | Min. | Max. |
|-----------|------|------|------|
| T1 | ms | 0.5 | 10 |
| T2 | ms | 0 | 200 |
| Т3 | ms | 0 | 200 |
| T7 | ms | 0 | 50 |
| T10 | ms | 0 | 500 |
| T11 | ms | 0 | 10 |
| T12 | ms | 150 | - |
| T13 | ms | 0 | - |
| T14 | ms | 0 | - |
| T15 | ms | 0 | - |
| T16 | ms | 0 | - |

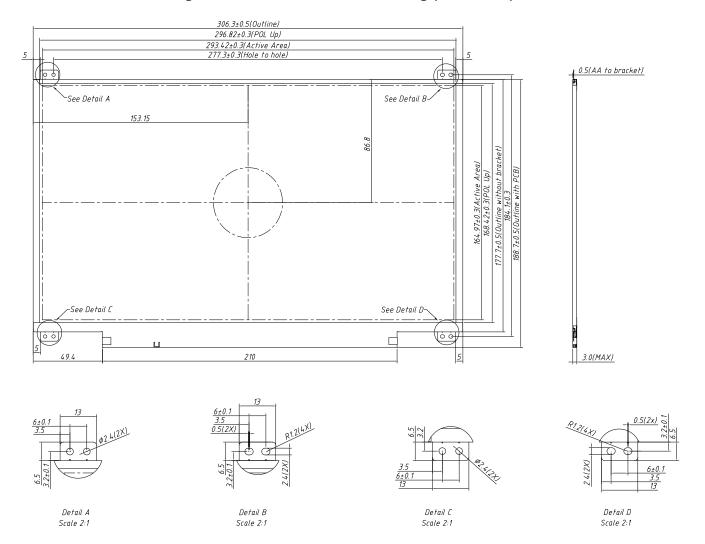


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10.0 Mechanical Characteristics

10.1Outline Drawing

Figure 16 Reference Outline Drawing (Front Side)





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Figure 17 Reference Outline Drawing (Back Side)





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10.2 Dimension Specifications

Table 14 Module Dimension Specifications

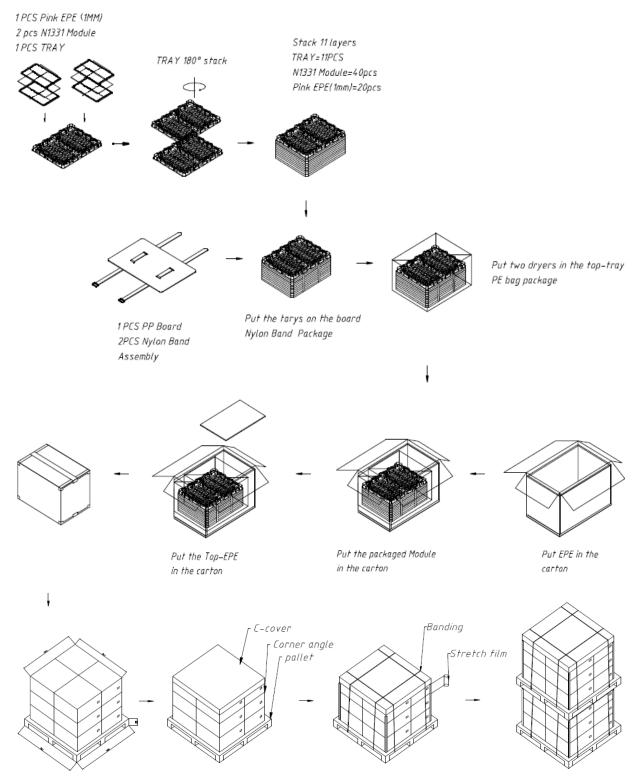
| | | - | | |
|-----------|-------|-------|-------|-------|
| Item | Min. | Тур. | Max. | Units |
| Width | 305.8 | 306.3 | 306.8 | mm |
| Length | 188.2 | 188.7 | 189.2 | mm |
| Thickness | - | 2.9 | 3.0 | mm |
| Weight | - | 244.6 | 260 | g |

Measure instrument: Vernier caliper



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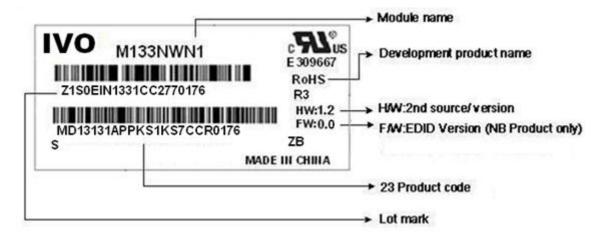
11.0 Package Specification (Tentative)





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12.0 Lot Mark



Lot Mark

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | | | | | | | | | | | | | | | |

code 1,2,4,5,6,7,8,9,10,11,16: IVO internal flow control code.

code 3: Production location.

code 12: Production year.

code 13: Production month.

code 14,15: Production date.

Code 17,18,19,20: Serial number.

Note (1) Production Year

| Year | 2,006 | 2,007 | 2,008 | 2,009 | 2,010 | 2,011 | 2,012 | 2,013 | 2,014 | 2,015 |
|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Mark | 6 | 7 | 8 | 9 | Α | В | С | D | E | F |

Note (2) Production Month

| Month | Jan. | Feb. | Mar. | Apr. | May. | Jun. | Jul. | Aug. | Sep. | Oct | Nov. | Dec. |
|-------|------|------|------|------|------|------|------|------|------|-----|------|------|
| Mark | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | Α | В | С |

1.1 23 Product Barcode

| 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 |
|--|
|--|

code 1,2:Manufacture District

code 3,4,5,6,7: IVO internal module name.

code 8,9,10,13,16: IVO internal flow control code.



| | | | | , , , , , , , , , , , , , , , , , , , | | |
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code 11,12: Cell location Suzhou defined as "SZ".

code 14,15: Module line kunshan defined as" KS".

code 17,18,19: Year, Month, Day Refer to Note(1) and Note(2) of Lot Mark.

code 20~23 : Serial Number.

13.0 General Precaution

13.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

13.2 Handling Precaution

- (1) Please mount LCD module by using mounting holes arranged in four corners tightly.
- (2) Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. IVO does not warrant the module, if customers disassemble or modify the module.
- (3) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid Crystal, and do not contact liquid crystal with skin. If liquid crystal contacts mouth or eyes, rinse out with water immediately. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and Rinse thoroughly with water.
- (4) Disconnect power supply before handling LCD module
- (5) Refrain from strong mechanical shock and /or any force to the module.
- (6) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature; etc otherwise LCD module may be damaged. It's recommended employing protection circuit for power supply.
- (7) Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when Persons handle the LCD module for incoming inspection or assembly.
- (8) When the surface is dusty, please wipe gently with absorbent cotton or other soft Material. When cleaning the adhesives, please use absorbent cotton wetted with a little Petroleum benzene or other adequate solvent.
- (9) Wipe off saliva or water drops as soon as possible. If saliva or water drops Contact with polarizer for a long time, they may causes deformation or color Fading.
- (10) Protection film must remove very slowly from the surface of LCD module to Prevent from electrostatic occurrence.
- (11) Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is Very weak to electrostatic discharge, Please be careful with electrostatic Discharge .Persons who handle the module should be grounded through adequate
- (12) Do not adjust the variable resistor located on the module.

13.3 Storage Precaution

- (1) Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
- (2) The module shall not be exposed under strong light such as direct sunlight. Otherwise, Display characteristics may be changed.
- (3) The module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.



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13.4 Operation Precaution

- (1) Do not connect or disconnect the module in the "Power On" condition.
- (2) Power supply should always be turned on/off by "Power on/off sequence"
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (4) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

13.5 Others

- (1) Ultra-violet ray filter is necessary for outdoor operation.
- (2) Avoid condensation of water which may result in improper operation or disconnection of electrode.
- (3) If the module keeps displaying the same pattern for a long period of time, the image may be "Sticked" to the screen.
- (4) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

13.6 Disposal

When disposing LCD module, obey the local environmental regulations.

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14.0 EDID Data Structure

| Address (DEC) | Address (HEX) | Field Name & Comments | Value (HEX) | Value (BIN) | Value (DEC) |
|------------------|------------------|--|----------------|----------------|----------------|
| 0 | 0 | Header | 00 | 00000000 | 0 |
| 1 | 1 | Header | FF | 11111111 | 255 |
| 2 | 2 | Header | FF | 11111111 | 255 |
| 3 | 3 | Header | FF | 11111111 | 255 |
| 4 | 4 | Header | FF | 11111111 | 255 |
| 5 | 5 | Header | FF | 11111111 | 255 |
| 6 | 6 | Header | FF | 11111111 | 255 |
| 7 | 7 | Header | 00 | 00000000 | 0 |
| 8 | 8 | manufacture code | 26 | 00100110 | 38 |
| 9 | 9 | manufacture code | CF | 11001111 | 207 |
| 10 | A | Product Code | 33 | 00110011 | 51 |
| 11 | В | Product Code | 05 | 00000101 | 5 |
| 12 | С | LCD module Serial No - ("0" if not used) | 00 | 00000000 | 0 |
| 13 | D | LCD module Serial No - ("0" if not used) | 00 | 00000000 | 0 |
| 14 | Е | LCD module Serial No - ("0" if not used) | 00 | 00000000 | 0 |
| 15 | F | LCD module Serial No - ("0" if not used) | 00 | 00000000 | 0 |
| 16 | 10 | Week of manufacture | 00 | 00000000 | 0 |
| 17 | 11 | Year of manufacture | 16 | 00010110 | 22 |
| 18 | 12 | EDID Structure Ver # = 1 | 01 | 00000001 | 1 |
| 19 | 13 | EDID revision # = 3 | 04 | 00000100 | 4 |
| 20 | 14 | Video I/P definition = Digital I/P (80h) | 80 | 10000000 | 128 |
| 21 | 15 | Max H image size = (Rounded to cm) | 1D | 00011101 | 29 |
| 22 | 16 | Max V image size = (Rounded to cm) | 11 | 00010001 | 17 |
| 23 | 17 | Display Gamma | 78 | 01111000 | 120 |



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| 24 | 18 | Feature support (no DPMS, Active off, RGB, timing BLK 1) | OA | 00001010 | 10 | |
| 25 | 19 | Red/Green Low bits (RxRy/GxGy) | 12 | 00010010 | 18 | |
| 26 | 1A | Blue/White Low bits (BxBy/WxWy) | 30 | 00110000 | 48 | |
| 27 | 1B | Red X Rx | 91 | 10010001 | 145 | |
| 28 | 1C | Red Y Ry | 56 | 01010110 | 86 | |
| 29 | 1D | Green X Gx | 53 | 01010011 | 83 | |
| 30 | 1E | Green Y Gy | 92 | 10010010 | 146 | |
| 31 | 1F | Blue X Bx | 28 | 00101000 | 40 | |
| 32 | 20 | Blue Y By | 1E | 00011110 | 30 | |
| 33 | 21 | White X Wx | 50 | 01010000 | 80 | |
| 34 | 22 | White Y Wy | 54 | 01010100 | 84 | |
| 35 | 23 | Established timings 1 (00h if not used) | 00 | 00000000 | 0 | |
| 36 | 24 | Established timing 2 (00h if not used) | 00 | 00000000 | 0 | |
| 37 | 25 | Manufacturer@39;s timings (00h if not used) | 00 | 00000000 | 0 | |
| 38 | 26 | Standard timing ID1 (01h if not used) | 01 | 00000001 | 1 | |
| 39 | 27 | Standard timing ID1 (01h if not used) | 01 | 00000001 | 1 | |
| 40 | 28 | Standard timing ID2 (01h if not used) | 01 | 00000001 | 1 | |
| 41 | 29 | Standard timing ID2 (01h if not used) | 01 | 00000001 | 1 | |
| 42 | 2A | Standard timing ID3 (01h if not used) | 01 | 00000001 | 1 | |
| 43 | 2B | Standard timing ID3 (01h if not used) | 01 | 00000001 | 1 | |
| 44 | 2C | Standard timing ID4 (01h if not used) | 01 | 00000001 | 1 | |
| 45 | 2D | Standard timing ID4 (01h if not used) | 01 | 00000001 | 1 | |
| 46 | 2E | Standard timing ID5 (01h if not used) | 01 | 00000001 | 1 | |
| 47 | 2F | Standard timing ID5 (01h if not used) | 01 | 00000001 | 1 | |
| 48 | 30 | Standard timing ID6 (01h if not used) | 01 | 00000001 | 1 | |
| 49 | 31 | Standard timing ID6 (01h if not used) | 01 | 00000001 | 1 | |
| 50 | 32 | Standard timing ID7 (01h if not used) | 01 | 00000001 | 1 | |
| 51 | 33 | Standard timing ID7 (01h if not used) | 01 | 00000001 | 1 | |
| 52 | 34 | Standard timing ID8 (01h if not used) | 01 | 00000001 | 1 | |



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| 53 | 35 | Standard timing ID8 (01h if n | Standard timing ID8 (01h if not used) | | 00000001 | 1 |
| 54 | 36 | Pixel Clock LSB | | D5 | 11010101 | 213 |
| 55 | 37 | Pixel Clock HSB | | 1C | 00011100 | 28 |
| 56 | 38 | Horizontal Active (lower 8 b | its) | 56 | 01010110 | 86 |
| 57 | 39 | Hor blanking (lower 8 bits) | | A6 | 10100110 | 166 |
| 58 | 3A | Horizontal Active/Horizontal (upper4:4 bits) | blanking | 50 | 01010000 | 80 |
| 59 | 3B | Vertcal active(lower 8 bits) | | 00 | 00000000 | 0 |
| 60 | 3C | Vertical blanking(lower 8 bi | ts) | 23 | 00100011 | 35 |
| 61 | 3D | Vertical Active : Vertical Bit (upper4:4 bits) | lanking | 30 | 00110000 | 48 |
| 62 | 3E | Horizontal Sync Offset | | 28 | 00101000 | 40 |
| 63 | 3F | Horizontal Sync Pulse Width | | 20 | 00100000 | 32 |
| 64 | 40 | Vertical Sync Offset , Sync V | Width | 3C | 00111100 | 60 |
| 65 | 41 | Horizontal Vertical Sync Offsupper 2 bits | set/Width | 00 | 00000000 | 0 |
| 66 | 42 | Horizontal Image Size | | 25 | 00100101 | 37 |
| 67 | 43 | Vertical image Size | | A5 | 10100101 | 165 |
| 68 | 44 | Horizontal Image Size / Verti | cal image | 10 | 00010000 | 16 |
| 69 | 45 | Horizontal Border = (0 for No LCD) | otebook | 00 | 00000000 | 0 |
| 70 | 46 | Vertical Border = (0 for Note | book LCD) | 00 | 00000000 | 0 |
| 71 | 47 | Non-interlaced, Normal, no see Separate sync, H/V pol Negativ | | 19 | 00011001 | 25 |
| 72 | 48 | Timing Descriptor #2 | | 00 | 00000000 | 0 |
| 73 | 49 | | | 00 | 00000000 | 0 |
| 74 | 4A | | | 00 | 00000000 | 0 |
| 75 | 4B | | | 00 | 00000000 | 0 |
| 76 | 4C | | | 00 | 00000000 | 0 |
| 77 | 4D | | | 00 | 00000000 | 0 |
| 78 | 4E | | | 00 | 00000000 | 0 |



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| 79 | 4F | | | 00 | 00000000 | 0 |
| 80 | 50 | | | 00 | 00000000 | 0 |
| 81 | 51 | | | 00 | 00000000 | 0 |
| 82 | 52 | | | 00 | 00000000 | 0 |
| 83 | 53 | | | 00 | 00000000 | 0 |
| 84 | 54 | | | 00 | 00000000 | 0 |
| 85 | 55 | | | 00 | 00000000 | 0 |
| 86 | 56 | | | 00 | 00000000 | 0 |
| 87 | 57 | | | 00 | 00000000 | 0 |
| 88 | 58 | | | 00 | 00000000 | 0 |
| 89 | 59 | | | 00 | 00000000 | 0 |
| 90 | 5A | Detailed timing/monitor desc | eriptor#3 | 00 | 00000000 | 0 |
| 91 | 5B | Flag | | 00 | 00000000 | 0 |
| 92 | 5C | Flag | | 00 | 00000000 | 0 |
| 93 | 5D | Range limits | | FE | 11111110 | 254 |
| 94 | 5E | Flag | | 00 | 00000000 | 0 |
| 95 | 5F | Min. Vertical Freq | | 49 | 01001001 | 73 |
| 96 | 60 | Max. Vertical Freq | | 6E | 01101110 | 110 |
| 97 | 61 | Min. Horizontal Freq | | 66 | 01100110 | 102 |
| 98 | 62 | Max.Horizontal Freq | | 6F | 01101111 | 111 |
| 99 | 63 | Max. Pixel Clock Freq | | 56 | 01010110 | 86 |
| 100 | 64 | | | 69 | 01101001 | 105 |
| 101 | 65 | | | 73 | 01110011 | 115 |
| 102 | 66 | | | 69 | 01101001 | 105 |
| 103 | 67 | | | 6F | 01101111 | 111 |
| 104 | 68 | | | 6E | 01101110 | 110 |
| 105 | 69 | New line character indicates | s end of | OA | 00001010 | 10 |
| 106 | 6A | | | 20 | 00100000 | 32 |
| 107 | 6B | | | 20 | 00100000 | 32 |
| 108 | 6C | Detailed timing/monitor desc | eriptor #4 | 00 | 00000000 | 0 |



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| 109 | 6D | | | 00 | 00000000 | 0 |
| 110 | 6E | | | 00 | 00000000 | 0 |
| 111 | 6F | FE (hex) defines ASCII s | tring | FE | 111111110 | 254 |
| 112 | 70 | Flag | | 00 | 00000000 | 0 |
| 113 | 71 | Manufacture P/N | | 4D | 01001101 | 77 |
| 114 | 72 | Manufacture P/N | | 31 | 00110001 | 49 |
| 115 | 73 | Manufacture P/N | | 33 | 00110011 | 51 |
| 116 | 74 | Manufacture P/N | | 33 | 00110011 | 51 |
| 117 | 75 | Manufacture P/N | | 4E | 01001110 | 78 |
| 118 | 76 | Manufacture P/N | | 57 | 01010111 | 87 |
| 119 | 77 | Manufacture P/N | | 4E | 01001110 | 78 |
| 120 | 78 | Manufacture P/N | | 31 | 00110001 | 49 |
| 121 | 79 | Manufacture P/N | | 20 | 00100000 | 32 |
| 122 | 7A | Manufacture P/N | | 52 | 01010010 | 82 |
| 123 | 7B | Manufacture P/N | | 33 | 00110011 | 51 |
| 124 | 7C | New line character indica | ates end of | 20 | 00100000 | 32 |
| 125 | 7D | | | OA | 00001010 | 10 |
| 126 | 7E | Extension Flag = 00 | | 00 | 00000000 | 0 |
| 127 | 7F | Checksum | | 5E | 01011110 | 94 |